SPECIFICATION AMENDMENTS

Page 1, amend the paragraph at lines 21 – 34, as follows:

There are many commercially successful non-volatile memory products being used today, particularly in the form of small cards, which use a flash EEPROM array of cells having a "split-channel" between source and drain diffusions. The floating gate of the cell is positioned over one portion of the channel and the word line (also referred to as a control gate) is positioned over the other channel portion as well as the floating gate. This effectively forms a cell with two transistors in series, one (the memory transistor) with a combination of the amount of charge on the floating gate and the voltage on the word line controlling the amount of current that can flow through its portion of the channel, and the other (the select transistor) having the word line alone serving as its gate. The word line extends over a row of floating gates. Examples of such cells, their uses in memory systems and methods of manufacturing them are given in United States patents nos. 5,070,032, 5,095,344, 5,315,541, 5,343,063, and 5,661,053, and in copending United States patent application serial no. 09/239,073, filed January 27, 1999, now patent no. 6,281,075, which patents ~~and application~~ are incorporated herein by this reference.

Page 5, amend the paragraph at lines 3 – 9, as follows:

Further examples of Dual Storage Element Cell arrays, in which the recessed select transistor gate element of the present invention may be implemented, are given in United States patents no. 6,103,573 and 6,151,248, and in pending applications serial nos. 09/667,344, filed September 22, 2000, now patent no. 6,512,263, and ~~—/———,———~~ 09/925,102, filed concurrently with the present application by Yuan et al., entitled "Scalable Self-Aligned Dual Floating Gate Memory Cell Array and Method of Forming the Array," which patents and patent applications are incorporated herein in their entirety by this reference.

Page 12, amend the paragraph at lines 2 – 23, as follows:

An example memory system incorporating the second and fourth embodiments of Figures 5A, 5B and 7A, 7B is generally illustrated in the block diagram of Figure 8. These are the embodiments that utilize steering gates extending along columns of floating gates. A large number of individually addressable memory cells according to the second and fourth specific embodiments are arranged in a regular array 111 of rows and columns, although other physical arrangements of cells are certainly possible. Bit lines, designated herein to extend along columns of the array 111 of cells, are electrically connected with a bit line decoder and driver circuit 113 through lines 115. Word lines, which are designated in this description to extend along rows of the array 111 of cells, are electrically connected through lines 117 to a word line decoder and driver circuit 119. Steering gates, which extend along columns of memory cells in the array 111, are electrically connected to a steering gate decoder and driver circuit 121 through lines 123. The steering gates and/or bit lines may be connected to their respective decoders by techniques described in a co-pending patent application by Harari *et al.* entitled "Steering Gate and Bit Line Segmentation in Non-Volatile Memories," serial no. 09/871,333, filed May 31, 2001, now patent no. 6,532,172, which application is incorporated herein in its entirety by this reference. Each of the decoders 113, 119 and 121 receives memory cell addresses over a bus 125 from a memory controller 127. The decoder and driving circuits are also connected to the controller 127 over respective control and status signal lines 129, 131 and 133. Voltages applied to the steering gates and bit lines are coordinated through a bus 122 that interconnects the decoder and driver circuits 113 and 121.

Page 13, amend the paragraph at lines 26 – 30, as follows:

Operation of memory systems such as those illustrated in Figures 8 and 9 are described in patents identified in the Background section above, and in other patents assigned to SanDisk Corporation, assignee of the present application. In addition, United States patent application serial no. 09/793,370, filed February 26, 2001, publication no. 2002/0118574, describes a data programming method, which application is incorporated herein by this reference.